# DPC-64-CTL-xxx Intelligent RF Transceiver Module

The extremely versatile DPC-64-CTL RF intelligent transceiver modules may be interfaced directly to any CMOS/ TTL serial data hosts such as microcontrollers and microprocessors to create a transparent bi-directional half duplex link. The DPC-64-CTL takes care of the RF communications protocol, eliminating the need for any special data formatting which is required for successful RF data communications. Simply input serial data in the format of 9600, 8,N,1 and the CTL will reproduce your original data at the receiving end. Error checking is automatically performed on the received data. The DPC-64-CTL is capable of transmitting 1-64 byte packets of data at a time. More than 64 bytes may easily be transmitted through simple implementation of the included optional flow control lines.

FEATURES

- **Transparent data formatting and error detection**
- **Processes 1 to 64 byte data packets per transmission**
- **Optional Handshaking lines included to transceive more than 64bytes**
- **Convenient Test Transmission Mode for diagnostic purposes**
- **9600 8,N,1 protocol compatible**
- **Simple to interface to CMOS/TTL hosts**
- **Significantly reduces design time**
- **Automatic TX/RX switching**
- **Automatic data input detection**
- **Available on 433.92, 868 and 914.5MHz**
- **Up to 700ft range**
- **5v operation, <15mA**
- **RF Carrier Detect Output**
- **Compatible with the DPC-64-RS232 modules**

MECHANICAL DIMENSIONS
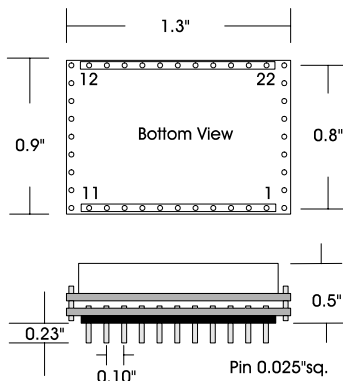
Pin Number	Description
1 to 7	No Connection
8	16MHz CLK output
9	TEST Link
10	Audio Output
11	Carrier Detect Output
12	+5V Supply
13,20, 22	GND
14	Send Data Control Line- Input
15	Data Ready Control Line- Output
16	Transmit Data– Output
17	Busy Control Line– Output
18	Receive Data– Input
19	Reserved– do not connect
21	Antenna

Detailed Pin Description

Pins 1-7

No connection.

Pin 8– CLK

This is a 16MHz external clock signal which may be interfaced to external devices if desired. Otherwise this pin may be left unconnected.

Pin 9– Test

This pin is internally pulled high via an internal pull-up resistor. When taken low, typically via a tactile feedback pushbutton switch or any other dry contact, the data input pin 18 will be ignored and a 64 byte internal preset message will be output on pin 16 of the receiving DPC-64-CTL module. The content of this test message will be:

<ABACOM Technologies> DPC-64 www.abacom-tech.com +1(416)236-3858

The test message is intended for diagnostic purposes and serves as a quick test to verify the integrity of the RF link. With a receiving host PC running a simple terminal program such as Hyperterminal configured for xx00,8,N,1 the content of the test message in a correctly configured RF wireless link will be displayed.

Alternatively, an LED connected to the Transmit Data Output pin 17 as shown in the test circuit will flash when a valid test message is received.

Pin 10– Audio Output

The analog signal on pin 10 is the demodulated signal from the receiver and is made available to the designer where it may be used for custom specific design functions. If not required, this pin may be left unconnected.

Pin 11– Carrier Detect

The CD pin is active low in the presence of an RF carrier. The CD may be used as additional control logic for external circuits. If not required, this pin may be left unconnected.

Pin12- +5V Supply

Supply pin 12 should be decoupled to Ground via a 0.1uF ceramic capacitor.

Pins 13,20,22– Supply/RF Ground

The three ground pins are internally connected to the DPC-64-CTL ground plane. We recommend connecting all three ground pins if possible. At a minimum any one of the ground pins must be connect to system ground. Pin 22 is preferred as an RF ground for 50 Ω coaxial cable feeding off board antenna.

Pin 14 – Send Data

The send data control line is active high. When taken high, the data received from the transmitting DPC-64-CTL will be serially output on pin 16. If held low, the data received over-the-air-will be stored in the DPC-64-CTL's buffer until "send data" is taken high. The send data line functions in association with the data ready pin 15.

Pin 15– Data Ready

When the receiving DPC-64 has received valid data, the data ready control line may be used to signal the receiving host that the DPC-64-CTL has valid data ready to upload. The receiving host then asserts a logic high level on the "send data" line at pin 14 and the data is uploaded.

Many applications require the received data from the DPC-64-CTL to be uploaded to the host without supervision. These applications therefore do not require interfacing the data ready control line and therefore the data ready pin 15 may be left unconnected and the send data pin 14 then simply tied high. In this configuration, the DPC-64-CTL will output the data as it is received.

Pin 16– Data Output

The data that has been transmitted from the DPC-64-CTL's is checked for errors by the receiving DPC-64CTL. Error free data will be output on pin 16 provided that the send data control line pin 14 is at a logic high level.

Pin 17– Busy

The busy control line goes high when the DPC-64-CTL transceiver module has either received its maximum of 64 bytes or when it has detected the end of incoming data (under conditions when < 64 bytes have been received from the

host).

The function of the busy line pin 17 is for data flow control with the host. Implementing the busy line is necessary in applications where more than 64 bytes are to be transmitted. Under these circumstances, the DPC-64-CTL transceiver module will receive the first 64 bytes of data, and then use the busy line to signal the host to pause sending further data until it is has completed its data processing functions and transmitted the data.

If the designers application does not require sending more than 64 bytes of data, then the busy control pin 16 may be left unconnected.

Pin 18– Data Input

Data to be transmitted over DPC-64-CTL RF link is fed into pin 18 in standard serial CMOS/TTL level data format of 9600bps, 8 data bits, No parity and one stop bit (9600,8,N,1). One to 64 bytes may be transmitted at a time without the need for the flow control as is implemented with the BUSY pin 17.

The DPC64-CTL transparently formats the data into the correct protocol for RF communications and then transmits the data received from the host.

When the host is not sending data to the DPC-64-CTL transceiver module, it is important that pin 18 is held high. If it is held low, the DPC-64-CTL will see this condition as valid data entering on pin 18 and will begin to transmit this erroneous data.

Pin 19– Reserved

Leave pin 19 unconnected. This pin is reserved for production purposes.
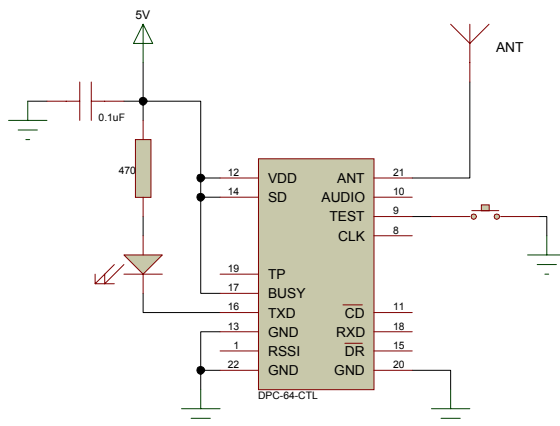
Pin 21– Antenna

A simple $\lambda/4$ whip antenna may be connected close to this pin. If a coaxial cable fed antenna is used, the core of the coax must be connect close to this pin, with the shield connected to the adjacent ground pins 20 or 22.

To calculate the physical length of a $\lambda/4$ antenna:

$\lambda/4 = 71.6 \div f$ meters
$\quad\; = 234 \div f$ feet

Where f = frequency (MHz)

Test Circuit (Two required to test a link)

When keying the TEST switch, the DPC-64-CTL will transmit its 64 byte preset test message to the receiving DPC-64-CTL test circuit. The test transmission will continue for as long as the test button is keyed.

The LED flashing at the **receiving** end serves as confirmation that the 64 byte message has been received, error free.

Electrical Characteristics

Parameter	Min	Typical	Max	Unit
Supply Voltage	4.5	5	5.5	Vdc
Current Consumption (TX ON)	22	26	32	mA
Current Consumption (RX ON)		12	15	mA
RX Section				
Receive Frequency		433.92		MHz
RF sensitivity, 1ppm BER		-100	-102	dBm
IF Passband		150		KHz
Interference Rejection at 20MHz		-100		dBm
RF spurious emissions into antenna		absent		
Output logic level: low		0.1		V
Output logic level: high		4		V
Carrier Detect threshold		-100		dBm
TX Section				
Transmit Frequency		433.92		MHz
FM Deviation		±25		KHz
Output power		10		dBm
Antenna Impedance		50		Ω
Operating Temperature	-10		+55	°C